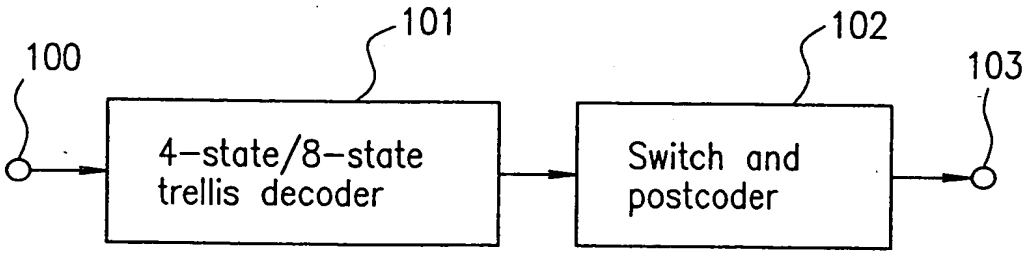
FIG. 1


100
101
4–state/8–state trellis decoder
102
Switch and postcoder
103

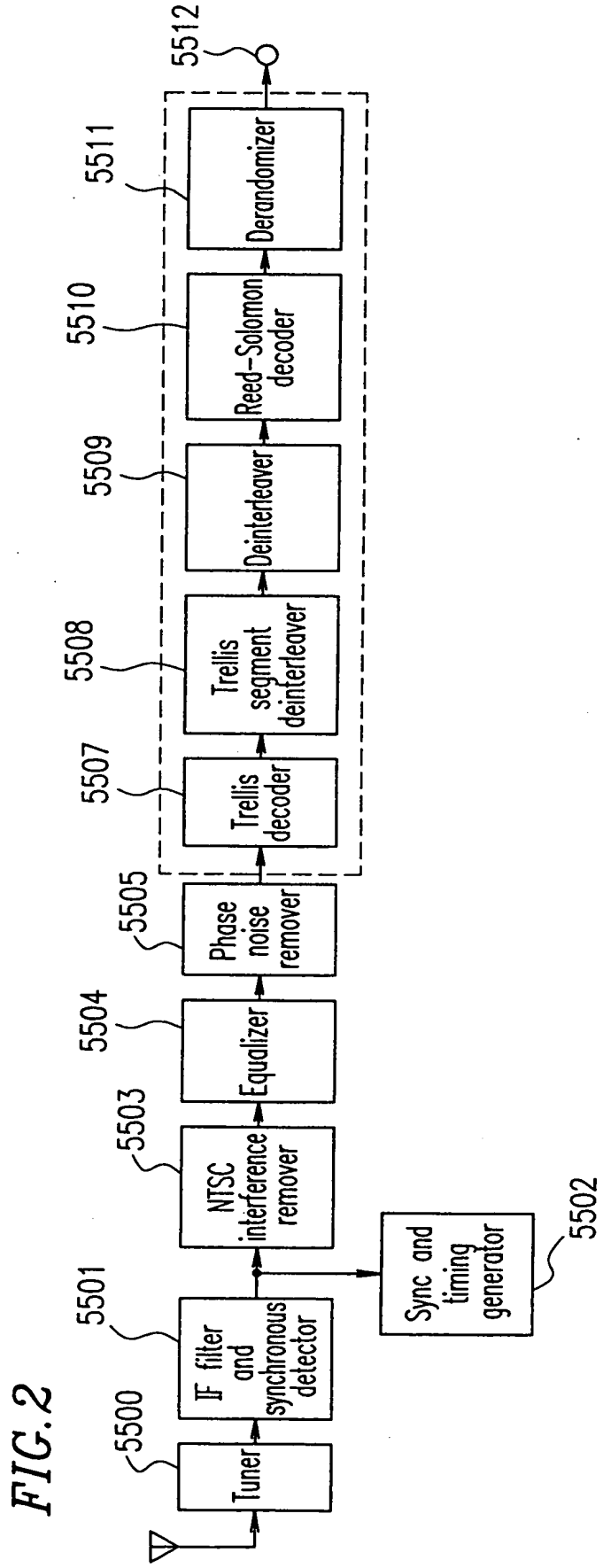

5500
Tuner
5501
IF filter and synchronous detector
5503
NTSC interference remover
5504
Equalizer
5505
Phase noise remover
5507
Trellis decoder
5508
Trellis segment deinterleaver
5509
Deinterleaver
5510
Reed-Solomon decoder
5511
Derandomizer
5512
Sync and timing generator
5502

FIG. 2

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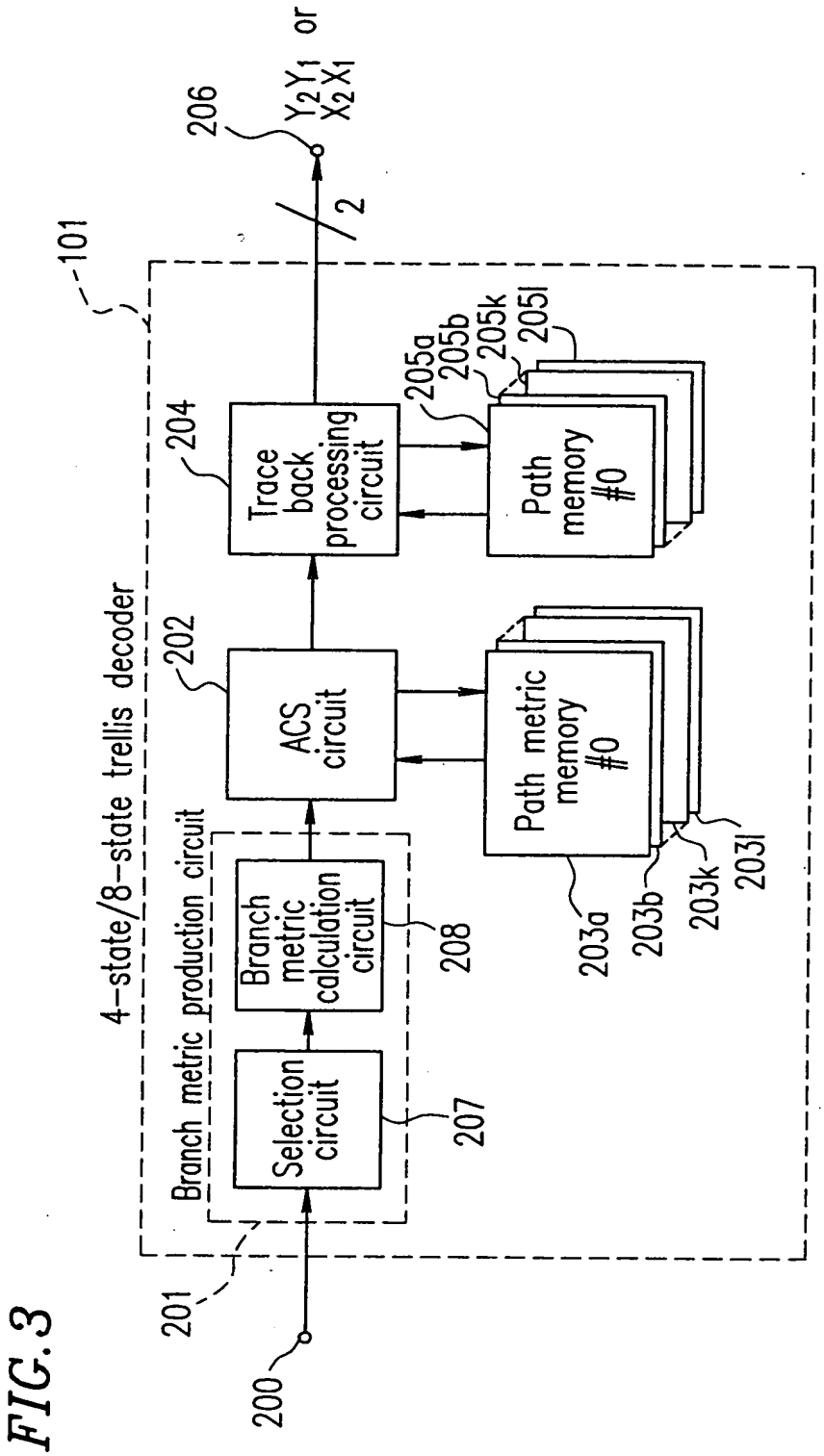

FIG. 3

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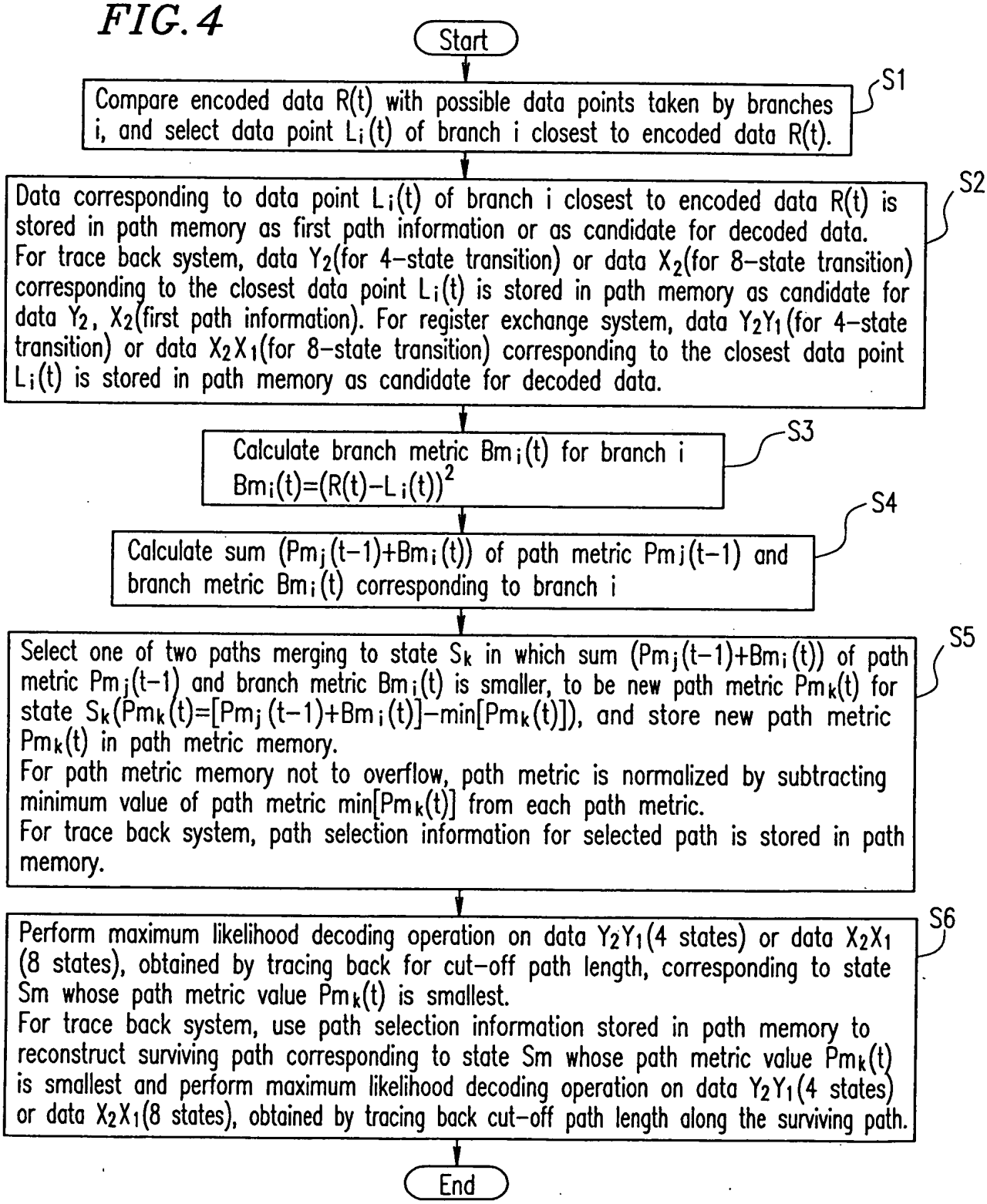
FIG. 4



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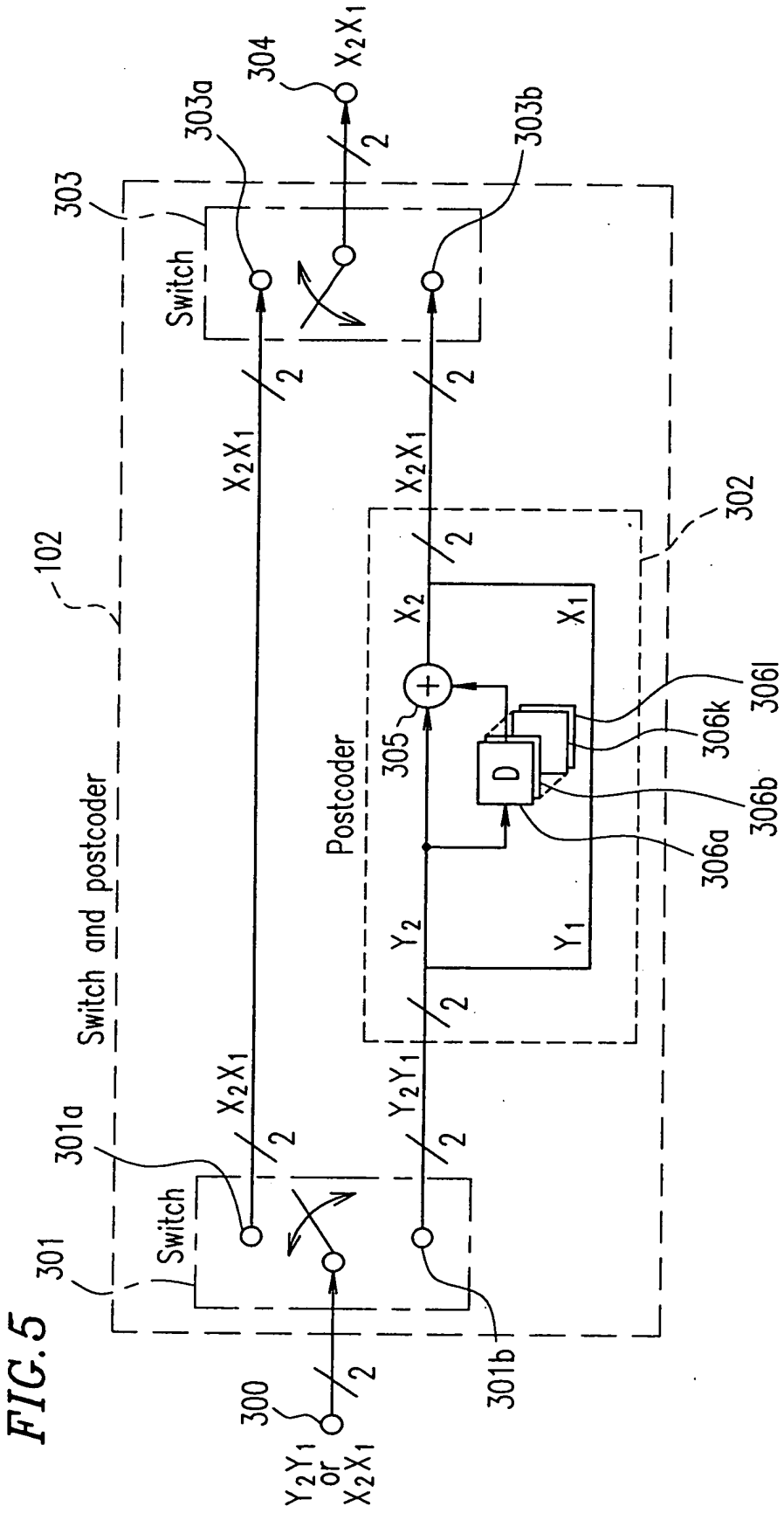

FIG. 5

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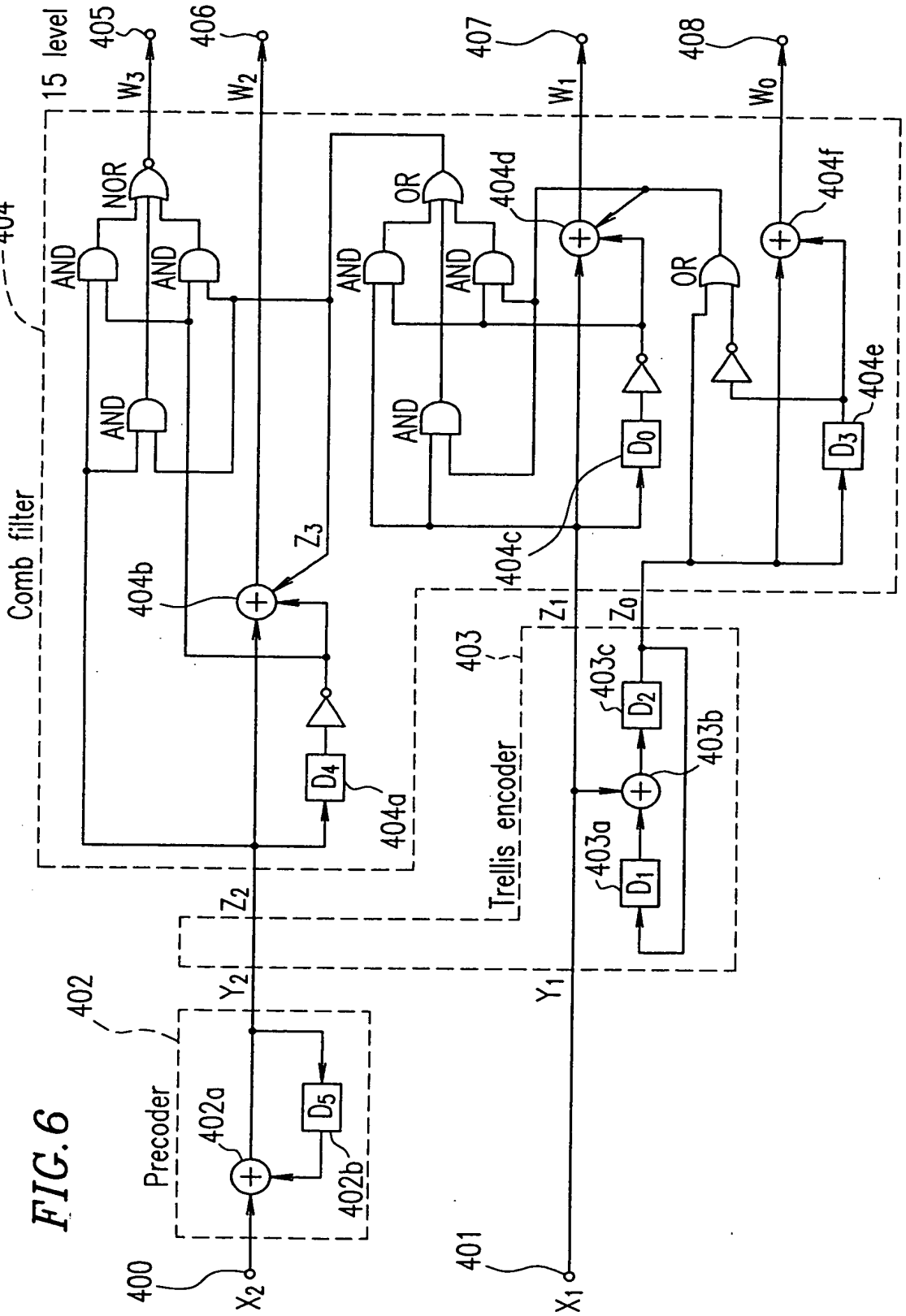

FIG. 6

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FIG. 7

4-state transition diagram

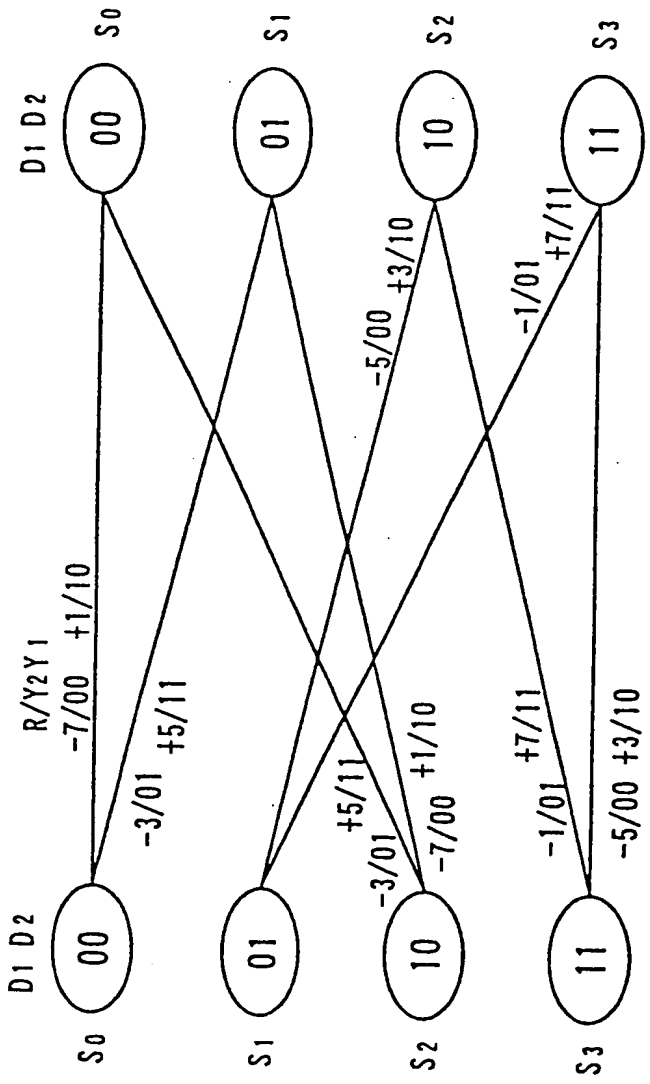

FIG. 8A

X_2	D_5 D_4	Y_2 Z_2	Z_3	W_3	W_2	Level
1	0	1	1	0	1	8,10,12,14
0	0	0	1	0	0	0,2,4,6
0	1	1	1	0	0	0,2,4,6
1	0	1	0	0	0	0,2,4,6
0	0	0	0	1	1	−8,−6,−4,−2
0	1	1	0	1	1	−8,−6,−4,−2
1	1	0	1	1	1	−8,−6,−4,−2
1	1	0	0	1	0	−14,−12,−10

FIG. 8B

Y_1 X_1	Z_3	W_1	W_0	Level
1	1	0	0	−8,0,8
0	1	0	0	−8,0,8
0	0	0	1	−14,−6,2,10
1	1	0	1	−14,−6,2,10
0	1	0	1	−14,−6,2,10
0	0	1	0	−12,−4,4,12
1	1	1	0	−12,−4,4,12
1	0	1	1	−10,−2,6,14
0	0	1	1	−10,−2,6,14
1	1	1	1	−10,−2,6,14

FIG. 9A

8-state transition diagram

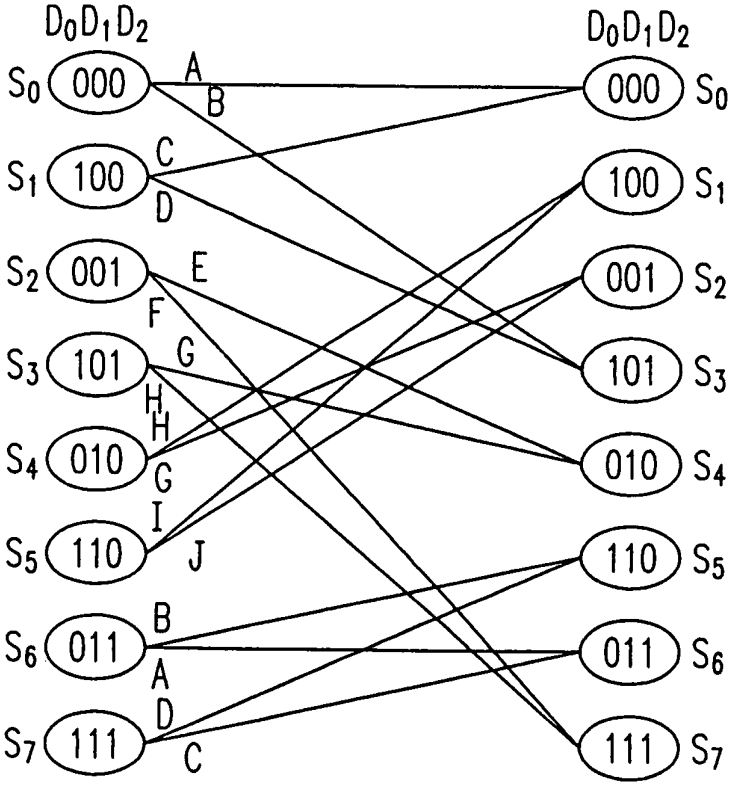

FIG. 9B

Level after being passed through comb filter

MAP				
L	W_3	W_2	W_1	W_0
+14	0	1	1	1
+12	0	1	1	0
+10	0	1	0	1
+8	0	1	0	0
+6	0	0	1	1
+4	0	0	1	0
+2	0	0	0	1
0	0	0	0	0
−2	1	1	1	1
−4	1	1	1	0
−6	1	1	0	1
−8	1	1	0	0
−10	1	0	1	1
−12	1	0	1	0
−14	1	0	0	1

FIG. 9C

L/X_2X_1 for respective branches

	L/X_2X_1
A	-8/10, 0/00, +8/10
B	-4/11, +4/01, +12/11
C	-12/10, -4/00, +4/10
D	-8/11, 0/01, +8/11
E	-6/10, +2/00, +10/10
F	-2/11, +6/01, +14/11
G	-10/10, -2/00, +6/10
H	-6/11, +2/01, +10/11
I	-10/11, -2/01, +6/11
J	-14/10, -6/00, +2/10

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Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

FIG. 9D

State transition diagram used commonly for 8-state transition and 4-state transition

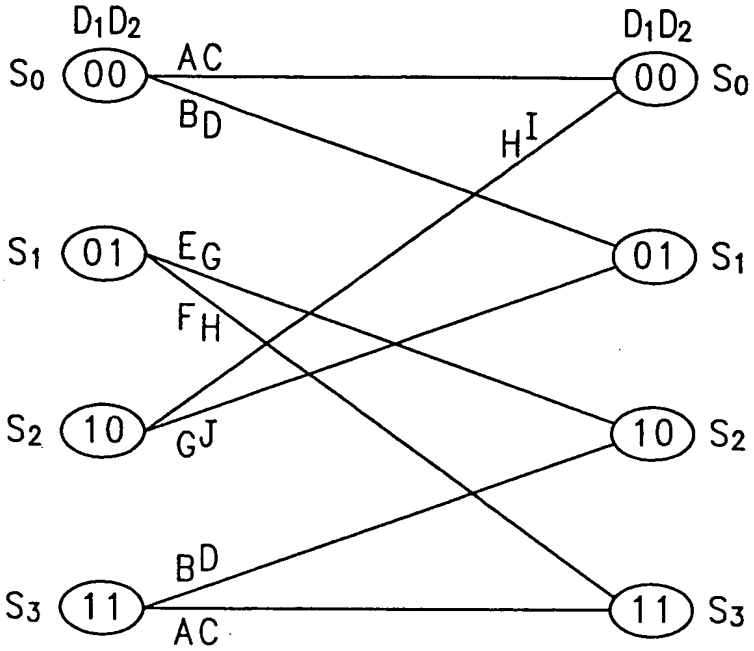

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FIG. 9E

L/X_2X_1 for respective branches

AC	−12 −8	−4 0	4 8
	10	00	10
BD	−8 −4	0 4	8 12
	11	01	11
EG	−10 −6	−2 2	6 10
	10	00	10
FH	−6 −2	2 6	10 14
	11	01	11
HI	−10 −6	−2 2	6 10
	11	01	11
GJ	−14 −10	−6 −2	2 6
	10	00	10

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Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

FIG. 10

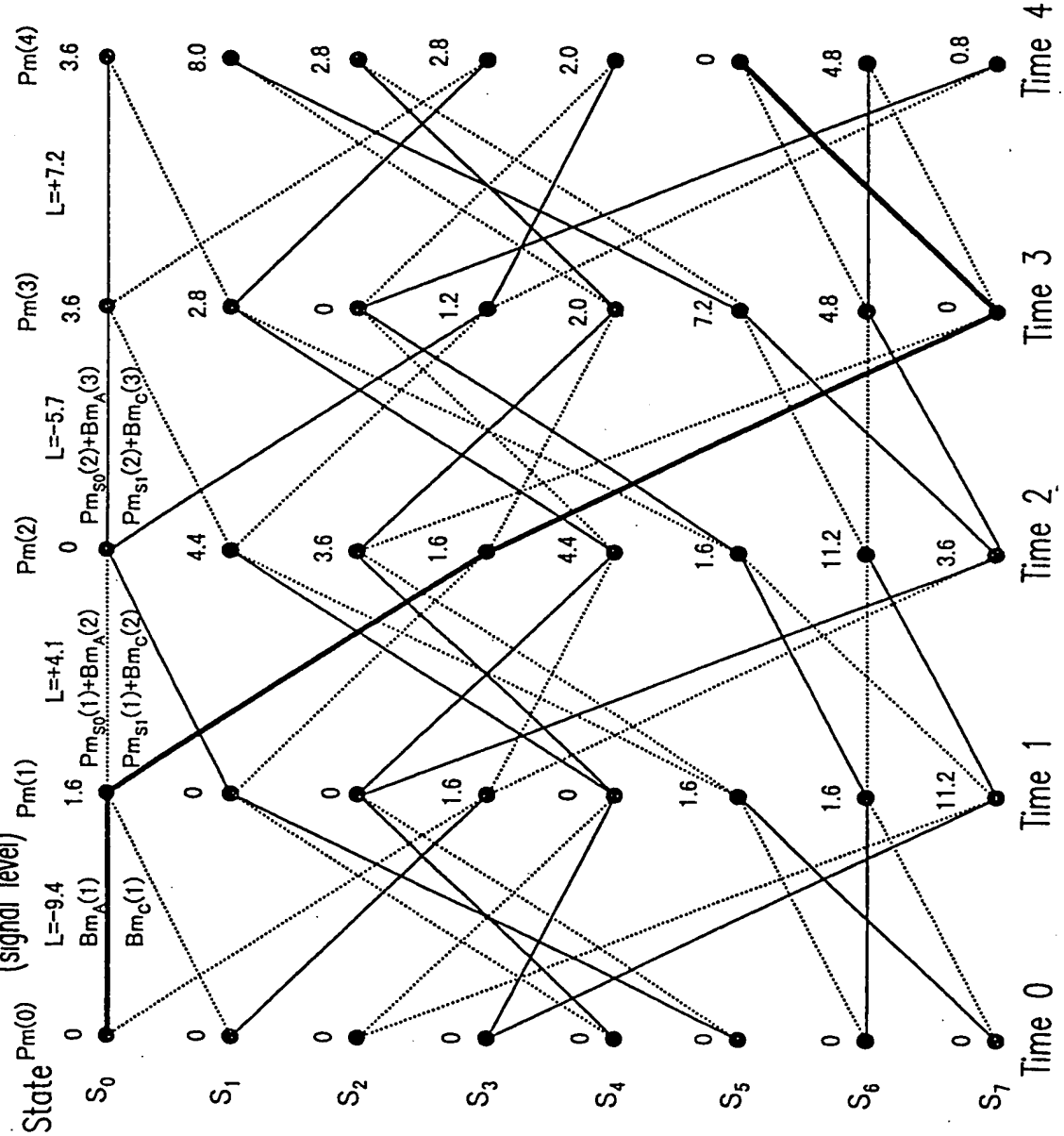

FIG. 11A

State transition from time 0 to time 1 (L=−9.4)

Branch metric	L/X_2X_1	X_1/coset
$Bm_A(1)=(-9.4-(-8))^2=1.96$	−8/10	0/UA
$Bm_B(1)=(-9.4-(-4))^2=29.16$	−4/11	1/UC2
$Bm_C(1)=(-9.4-(-12))^2=6.76$	−12/10	0/UC1
$Bm_D(1)=(-9.4-(-8))^2=1.96$	−8/11	1/UA
$Bm_E(1)=(-9.4-(-6))^2=11.56$	−6/10	0/UD2
$Bm_F(1)=(-9.4-(-2))^2=54.76$	−2/11	1/UB2
$Bm_G(1)=(-9.4-(-10))^2=0.36$	−10/10	0/UB1
$Bm_H(1)=(-9.4-(-6))^2=11.56$	−6/11	1/UD2
$Bm_I(1)=(-9.4-(-10))^2=0.36$	−10/11	1/UB1
$Bm_J(1)=(-9.4-(-6))^2=11.56$	−6/00	0/UD1

FIG. 11B

State	Comparison of path metric (Pm(0)+Bm(1)=Bm(1), where Pm(0)=0)	Path metric Pm(1)
S_0	$Bm_A(1)=1.96 < Bm_C(1)=6.76$	$Pm_{S0}(1)=1.96-0.36=1.6$
S_1	$Bm_H(1)=11.56 > Bm_I(1)=\underline{0.36}$	$Pm_{S1}(1)=0.36-0.36=0$
S_2	$Bm_G(1)=\underline{0.36} < Bm_J(1)=11.56$	$Pm_{S2}(1)=0.36-0.36=0$
S_3	$Bm_B(1)=29.16 > Bm_D(1)=1.96$	$Pm_{S3}(1)=1.96-0.36=1.6$
S_4	$Bm_E(1)=11.56 > Bm_G(1)=\underline{0.36}$	$Pm_{S4}(1)=0.36-0.36=0$
S_5	$Bm_B(1)=29.16 > Bm_D(1)=1.96$	$Pm_{S5}(1)=1.96-0.36=1.6$
S_6	$Bm_A(1)=1.96 < Bm_C(1)=6.76$	$Pm_{S6}(1)=1.96-0.36=1.6$
S_7	$Bm_F(1)=54.76 > Bm_H(1)=11.56$	$Pm_{S7}(1)=11.56-0.36=11.2$

State transition from time 1 to time 2 (L=+4.1)

FIG. 12A

Branch metric	L/X_2X_1	X_1/coset
$Bm_A(2)=(+4.1-(+8))^2=15.21$	+8/10	0/UA
$Bm_B(2)=(+4.1-(+4))^2=0.01$	+4/01	1/UC2
$Bm_C(2)=(+4.1-(+4))^2=0.01$	+4/10	0/UC1
$Bm_D(2)=(+4.1-(+8))^2=15.21$	+8/11	1/UA
$Bm_E(2)=(+4.1-(+2))^2=4.41$	+2/00	0/UD2
$Bm_F(2)=(+4.1-(+6))^2=3.61$	+6/01	1/UB2
$Bm_G(2)=(+4.1-(+6))^2=3.61$	+6/10	0/UB1
$Bm_H(2)=(+4.1-(+2))^2=4.41$	+2/01	1/UD2
$Bm_I(2)=(+4.1-(+6))^2=3.61$	+6/11	1/UB1
$Bm_J(2)=(+4.1-(+2))^2=4.41$	+2/10	0/UD1

FIG. 12B

State	Comparison of path metric (Pm(1)+Pm(2))	Path metric Pm(2)
S_0	$Pms_0(1)+Bm_A(2)=16.81 > Pms_1(1)+Bm_C(2)=\underline{0.01}$	$Pms_0(2)=0.01-0.01=0$
S_1	$Pms_4(1)+Bm_H(2)=4.41 < Pms_5(1)+Bm_I(2)=5.21$	$Pms_1(2)=4.41-0.01=4.4$
S_2	$Pms_4(1)+Bm_G(2)=3.61 < Pms_5(1)+Bm_J(2)=6.01$	$Pms_2(2)=3.61-0.01=3.6$
S_3	$Pms_0(1)+Bm_B(2)=1.61 < Pms_1(1)+Bm_D(2)=15.21$	$Pms_3(2)=1.61-0.01=1.6$
S_4	$Pms_2(1)+Bm_E(2)=4.41 < Pms_3(1)+Bm_G(2)=5.21$	$Pms_4(2)=4.41-0.01=4.4$
S_5	$Pms_6(1)+Bm_B(2)=1.61 < Pms_7(1)+Bm_D(2)=26.41$	$Pms_5(2)=1.61-0.01=1.6$
S_6	$Pms_6(1)+Bm_A(2)=16.81 > Pms_7(1)+Bm_C(2)=11.21$	$Pms_6(2)=11.21-0.01=11.2$
S_7	$Pms_2(1)+Bm_F(2)=3.61 < Pms_3(1)+Bm_H(2)=6.01$	$Pms_7(2)=3.61-0.01=3.6$

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State transition from time 2 to time 3 (L=-5.7)

FIG. 13A

Branch metric	L/X_2X_1	X_1/coset
$Bm_A(2)=(-5.7-(-8))^2=5.29$	-8/10	0/UA
$Bm_B(2)=(-5.7-(-4))^2=2.89$	-4/11	1/UC2
$Bm_C(2)=(-5.7-(-4))^2=2.89$	-4/00	0/UC1
$Bm_D(2)=(-5.7-(-8))^2=5.29$	-8/11	1/UA
$Bm_E(2)=(-5.7-(-6))^2=0.09$	-6/10	0/UD2
$Bm_F(2)=(-5.7-(-2))^2=13.69$	-2/11	1/UB2
$Bm_G(2)=(-5.7-(-2))^2=13.69$	-2/10	0/UB1
$Bm_H(2)=(-5.7-(-6))^2=0.09$	-6/11	1/UD2
$Bm_I(2)=(-5.7-(-2))^2=13.69$	-2/01	1/UB1
$Bm_J(2)=(-5.7-(-6))^2=0.09$	-6/00	0/UD1

FIG. 13B

State	Comparison of path metric (Pm(2)+Pm(3))	Path metric Pm(3)
S_0	$Pms_0(2)+Bm_A(3)=5.29 < Pms_1(2)+Bm_C(3)=7.29$	$Pms_0(3)=5.29-1.69=3.6$
S_1	$Pms_4(2)+Bm_H(3)=4.49 < Pms_5(2)+Bm_I(3)=15.29$	$Pms_1(3)=4.49-1.69=2.8$
S_2	$Pms_4(2)+Bm_G(3)=18.09 > Pms_5(2)+Bm_J(3)=\underline{1.69}$	$Pms_2(3)=1.69-1.69=0$
S_3	$Pms_0(2)+Bm_B(3)=2.89 < Pms_1(2)+Bm_D(3)=9.69$	$Pms_3(3)=2.89-1.69=1.2$
S_4	$Pms_2(2)+Bm_E(3)=3.69 < Pms_3(2)+Bm_G(3)=15.29$	$Pms_4(3)=3.69-1.69=2.0$
S_5	$Pms_6(2)+Bm_B(3)=14.09 > Pms_7(2)+Bm_D(3)=8.89$	$Pms_5(3)=8.89-1.69=7.2$
S_6	$Pms_6(2)+Bm_A(3)=16.49 > Pms_7(2)+Bm_C(3)=6.49$	$Pms_6(3)=6.49-1.69=4.8$
S_7	$Pms_2(2)+Bm_F(3)=17.29 > Pms_3(2)+Bm_H(3)=\underline{1.69}$	$Pms_7(3)=1.69-1.69=0$

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State transition from time 3 to time 4 (L=+7.2)

FIG. 14A

Branch metric	L/X_2X_1	X_1/coset
$Bm_A(4)=(+7.2-(+8))^2=0.64$	+8/10	0/UA
$Bm_B(4)=(+7.2-(+4))^2=10.24$	+4/01	1/UC2
$Bm_C(4)=(+7.2-(+4))^2=10.24$	+4/10	0/UC1
$Bm_D(4)=(+7.2-(+8))^2=0.64$	+8/11	1/UA
$Bm_E(4)=(+7.2-(+10))^2=7.84$	+10/10	0/UD2
$Bm_F(4)=(+7.2-(+6))^2=1.44$	+6/01	1/UB2
$Bm_G(4)=(+7.2-(+6))^2=1.44$	+6/10	0/UB1
$Bm_H(4)=(+7.2-(+10))^2=7.84$	+10/11	1/UD2
$Bm_I(4)=(+7.2-(+6))^2=1.44$	+6/11	1/UB1
$Bm_J(4)=(+7.2-(+2))^2=27.04$	+2/10	0/UD1

FIG. 14B

State	Comparison of path metric (Pm(3)+Pm(4))	Path metric Pm(4)
S_0	$Pms_0(3)+Bm_A(4)=4.24 < Pms_1(3)+Bm_C(4)=13.04$	$Pms_0(4)=4.24-0.64=3.6$
S_1	$Pms_4(3)+Bm_H(4)=9.84 > Pms_5(3)+Bm_I(4)=8.64$	$Pms_1(4)=8.64-0.64=8.0$
S_2	$Pms_4(3)+Bm_G(4)=3.44 < Pms_5(3)+Bm_J(4)=34.24$	$Pms_2(4)=3.44-0.64=2.8$
S_3	$Pms_0(3)+Bm_B(4)=13.84 > Pms_1(3)+Bm_D(4)=3.44$	$Pms_3(4)=3.44-0.64=2.8$
S_4	$Pms_2(3)+Bm_E(4)=7.84 > Pms_3(3)+Bm_G(4)=2.64$	$Pms_4(4)=2.64-0.64=2.0$
S_5	$Pms_6(3)+Bm_B(4)=15.04 > Pms_7(3)+Bm_D(4)=\underline{0.64}$	$Pms_5(4)=0.64-0.64=0$
S_6	$Pms_6(3)+Bm_A(4)=5.44 < Pms_7(3)+Bm_C(4)=10.24$	$Pms_6(4)=5.44-0.64=4.8$
S_7	$Pms_2(3)+Bm_F(4)=1.44 < Pms_3(3)+Bm_H(4)=9.04$	$Pms_7(4)=1.44-0.64=0.8$

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Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

FIG. 15A 8-state transition diagram

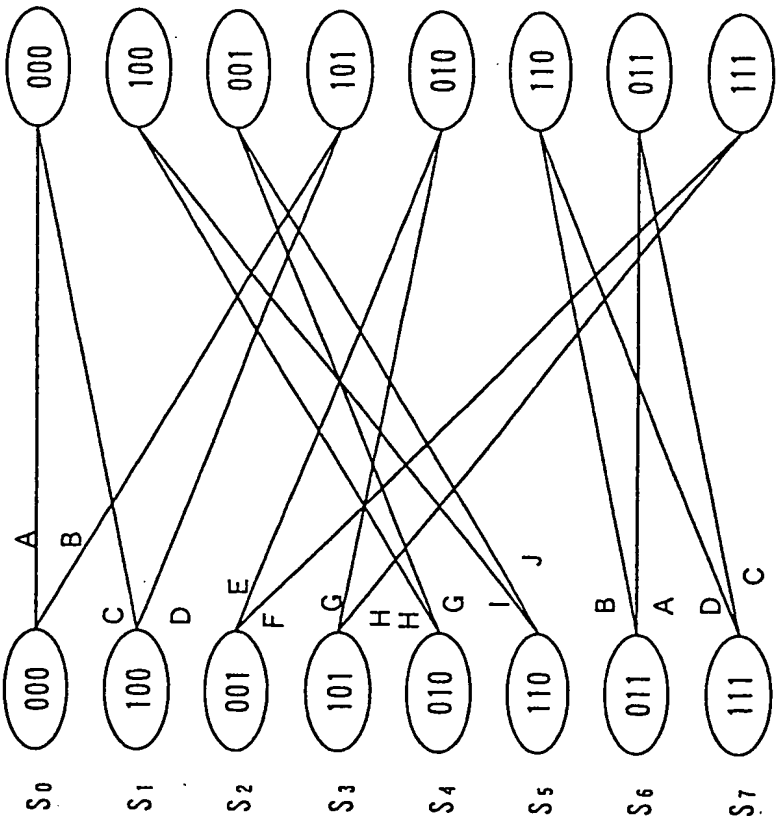

FIG. 15B Relationship between levels after being passed through comb filter and cosets

Coset	Level
UA	+8, 0, −8
UB1	+6, −2, −10
UB2	+14, +6, −2
UC1	+4, −4, −12
UC2	+12, +4, −4
UD1	+2, −6, −14
UD2	+10, +2, −6

FIG. 15C X_1/coset for respective branches

	X_1/coset
A	0/UA
B	1/UC2
C	0/UC1
D	1/UA
E	0/UD2
F	1/UB2
G	0/UB1
H	1/UD2
I	1/UB1
J	0/UD1

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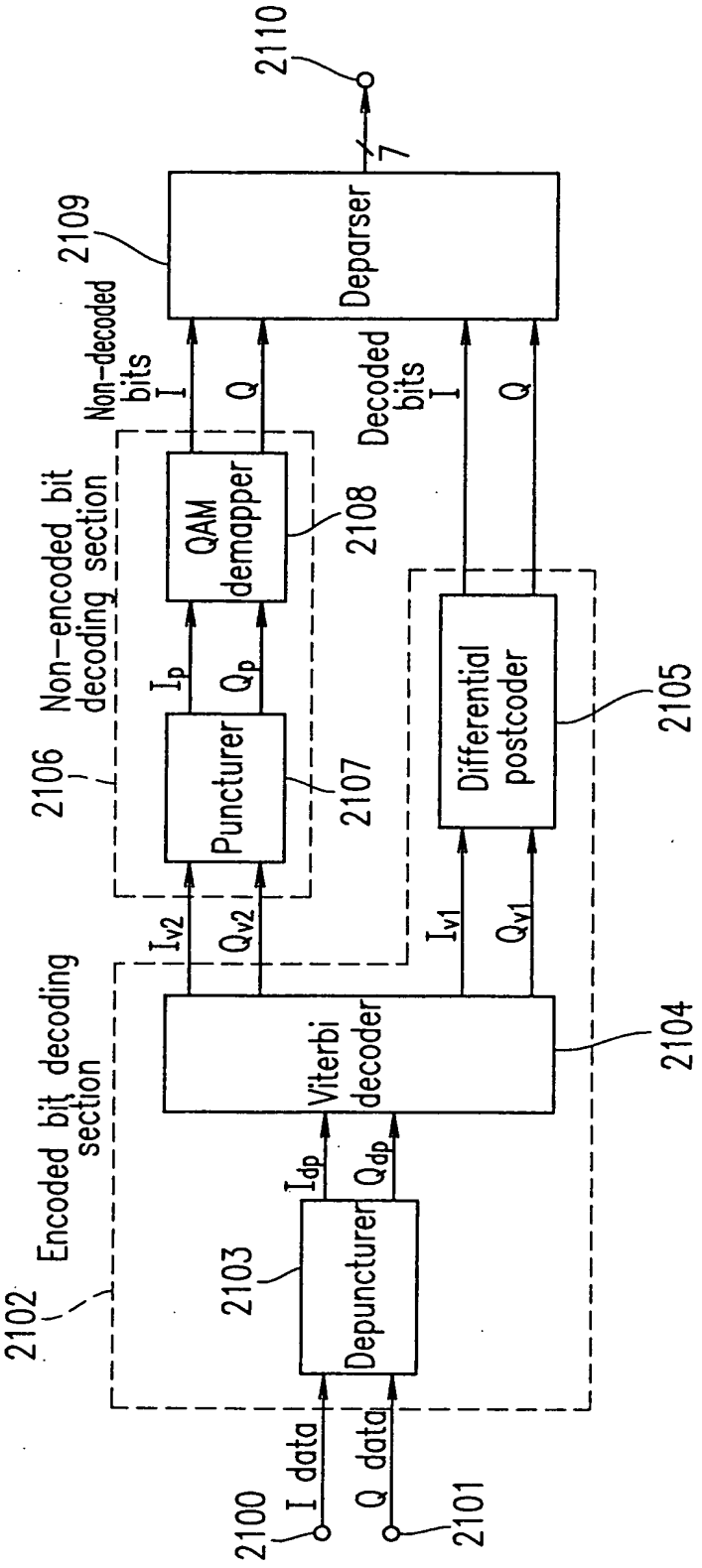
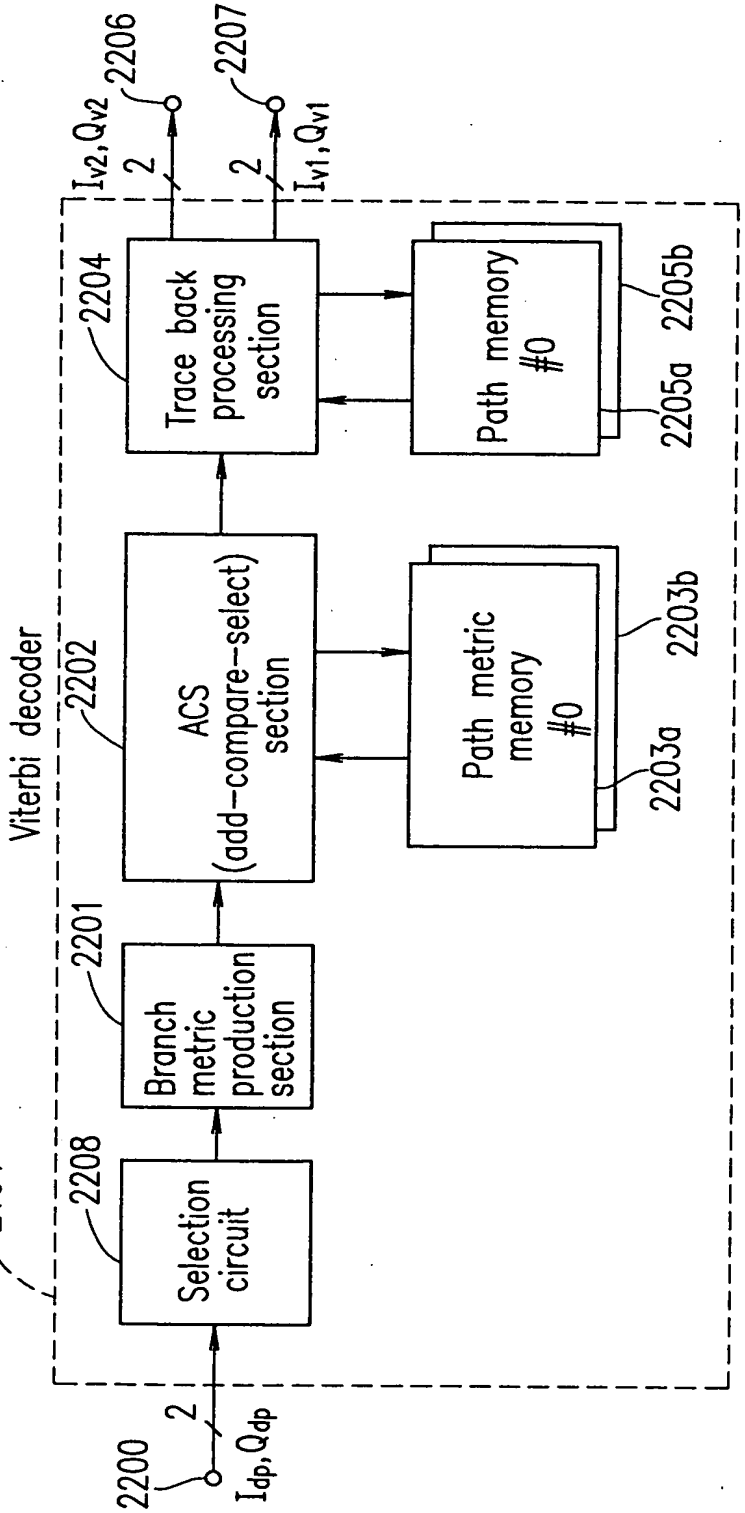


FIG. 16

FIG. 17


2104
Viterbi decoder
2200
2
I_{dp}, Q_{dp}
2208
Selection circuit
2201
Branch metric production section
2202
ACS (add-compare-select) section
2203a
Path metric memory #0
2203b
2204
Trace back processing section
2205a
Path memory #0
2205b
2206
2207
I_{v2}, Q_{v2}
I_{v1}, Q_{v1}

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Express Label No.: EV351884480US

FIG. 18A State transition diagram

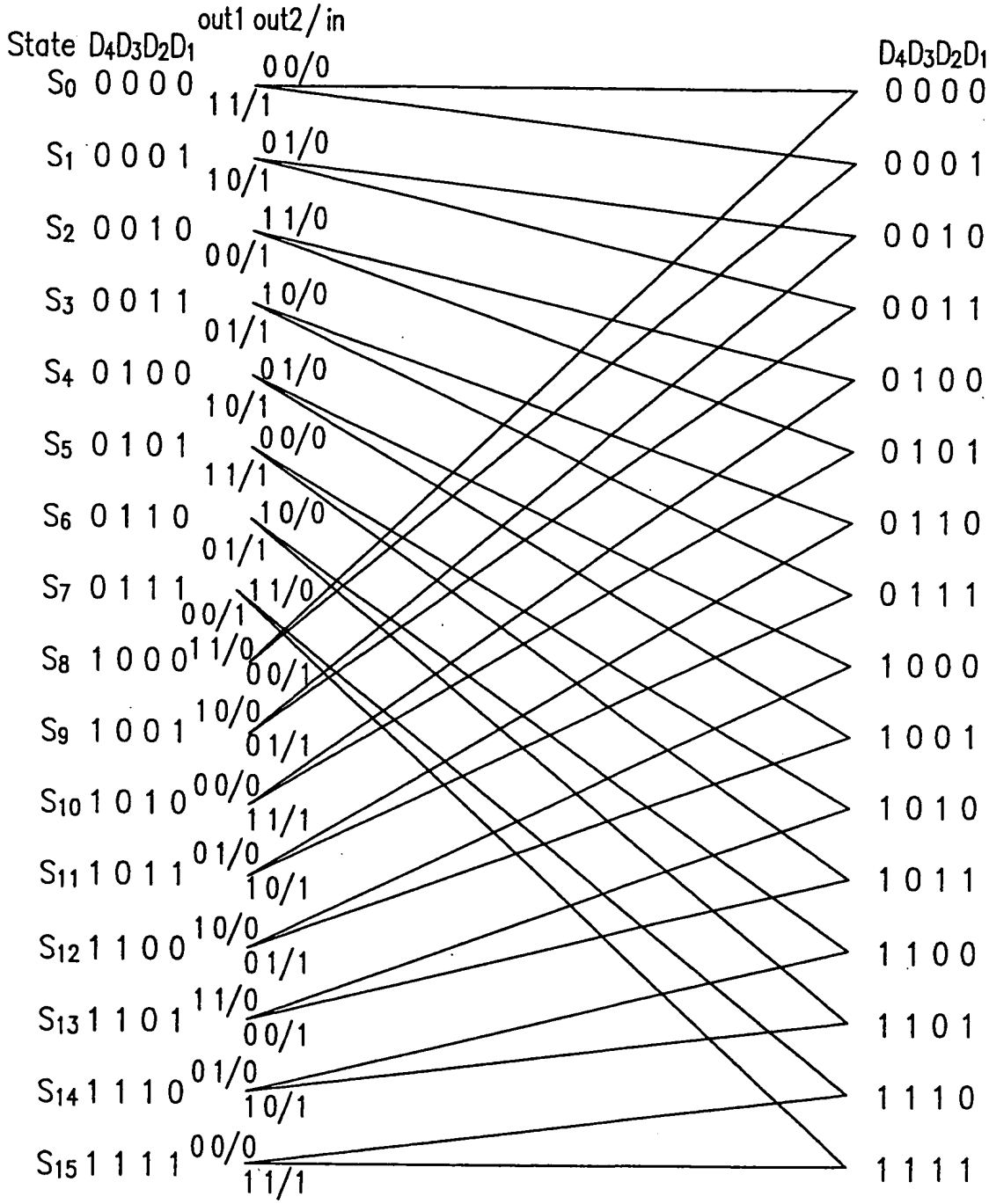
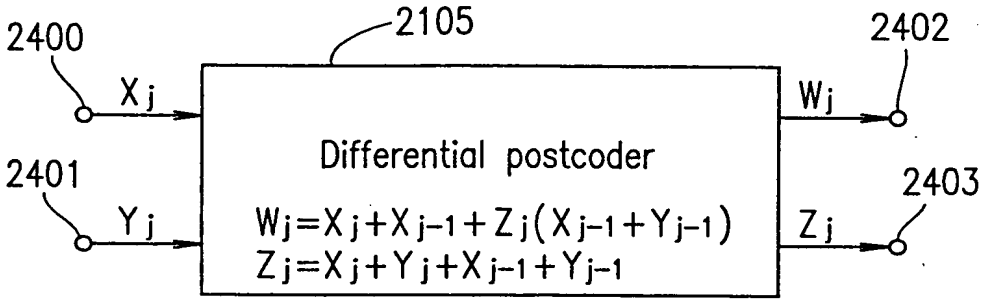


FIG. 18B Relationship between out1,out2 and signal level

out1,out2	Signal level
0	−7,−3,+1,+5
1	−5,−1,+3,+7

FIG. 19


2400
2105
2402
Xj
Wj
Differential postcoder
2401
2403
Yj
Wj=Xj+Xj-1+Zj(Xj-1+Yj-1)
Zj
Zj=Xj+Yj+Xj-1+Yj-1

Inventor(s): Hiroyuki Senda, et al.
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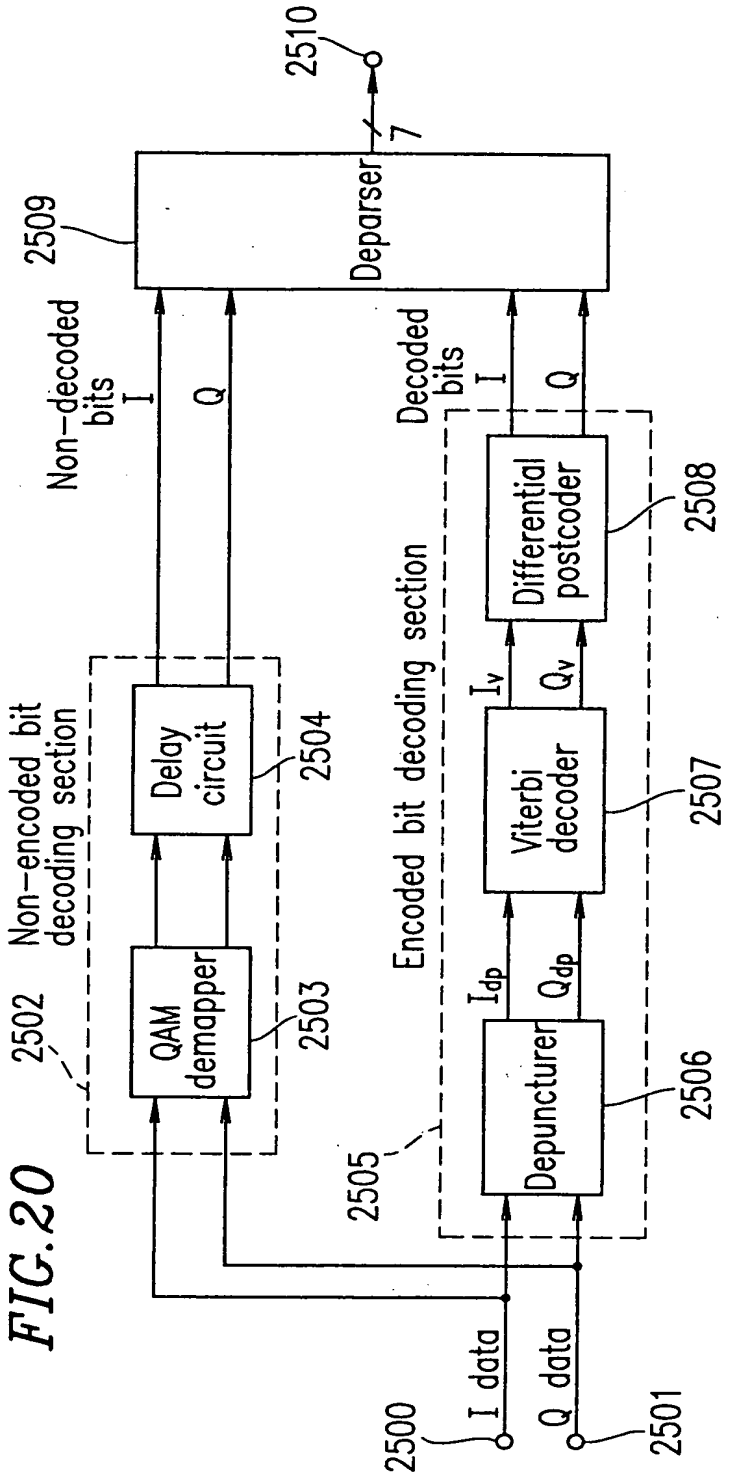

FIG. 20

FIG.21A Arrangement of 64QAM encoding points

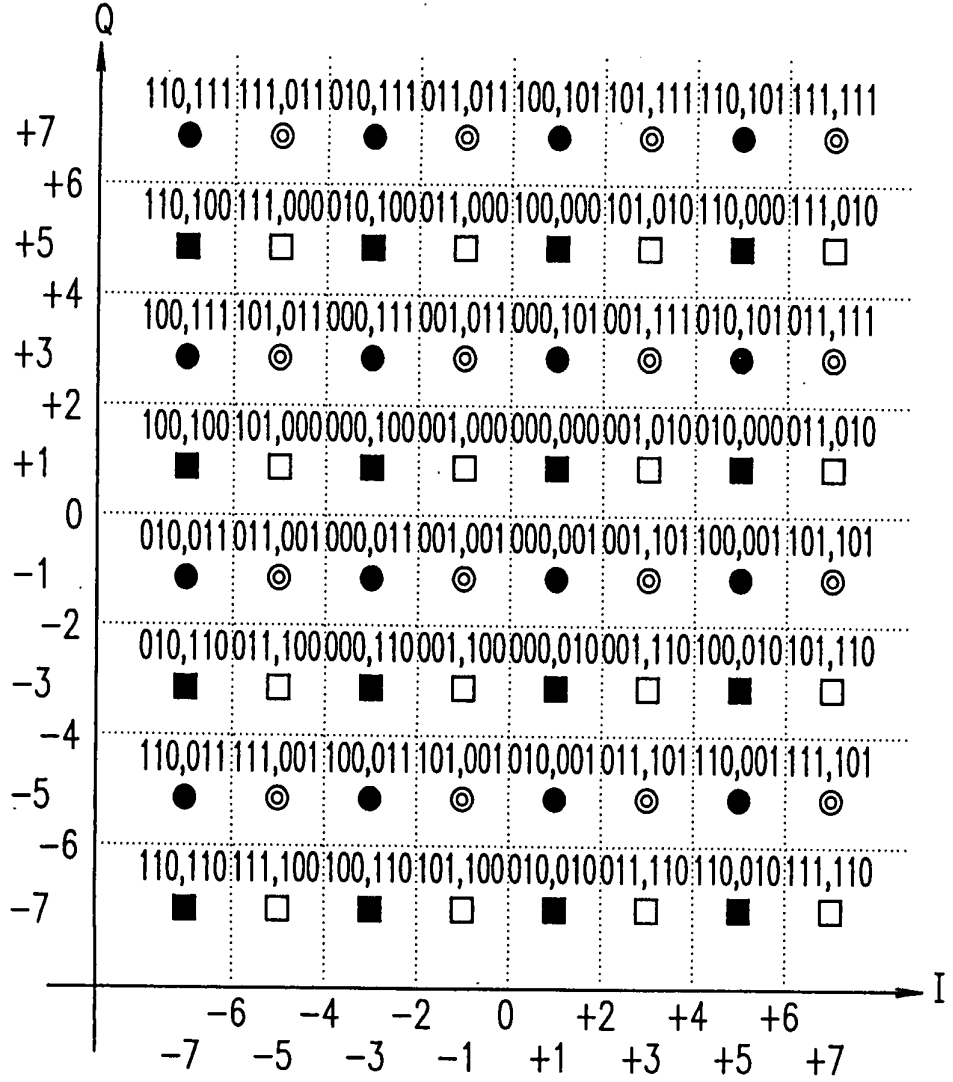

FIG.21B Encoding point

I bit			Q bit		
MSB					LSB
(C(1)	C(2)	C(3)	, C(4)	C(5)	C(6))

FIG.21C

Encoded bits C(3),C(6)

	C(3)	C(6)
●	0	1
■	0	0
□	1	0
◎	1	1

"0" → −7,−3,+1,+5

"1" → −5,−1,+3,+7

Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
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Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

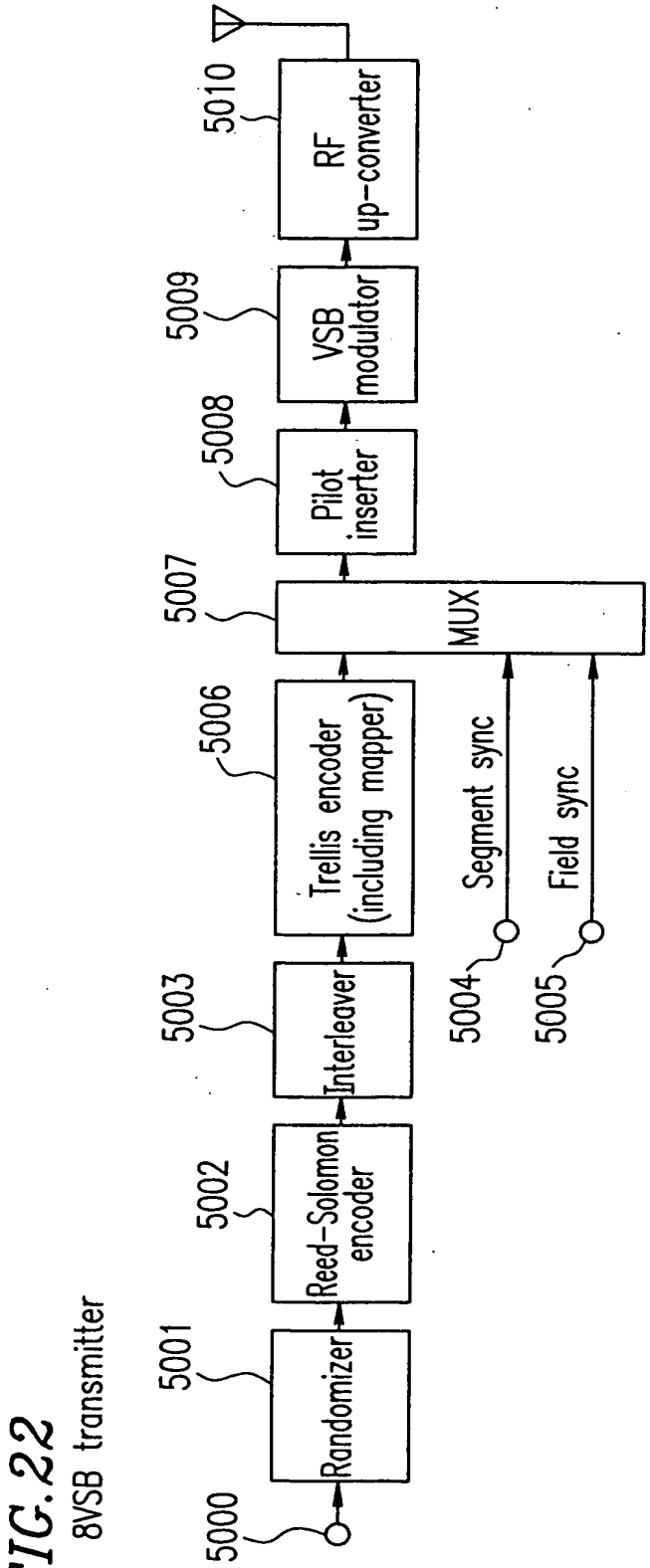

FIG.22
8VSB transmitter

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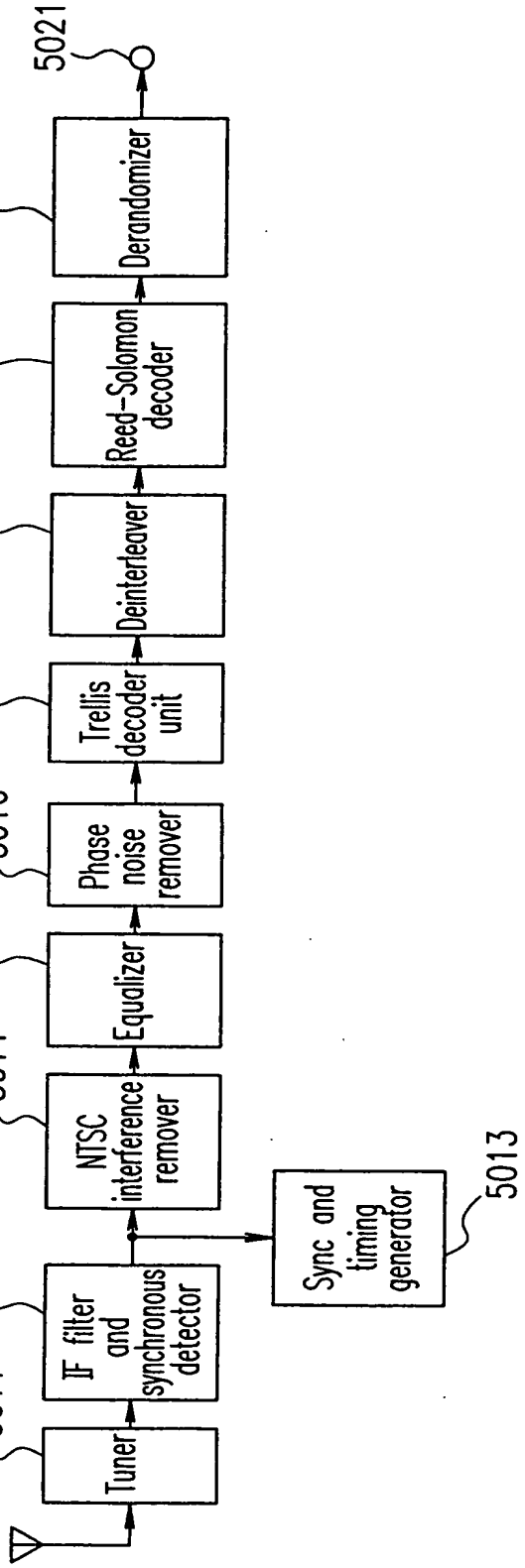
FIG. 23

8VSB receiver



Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

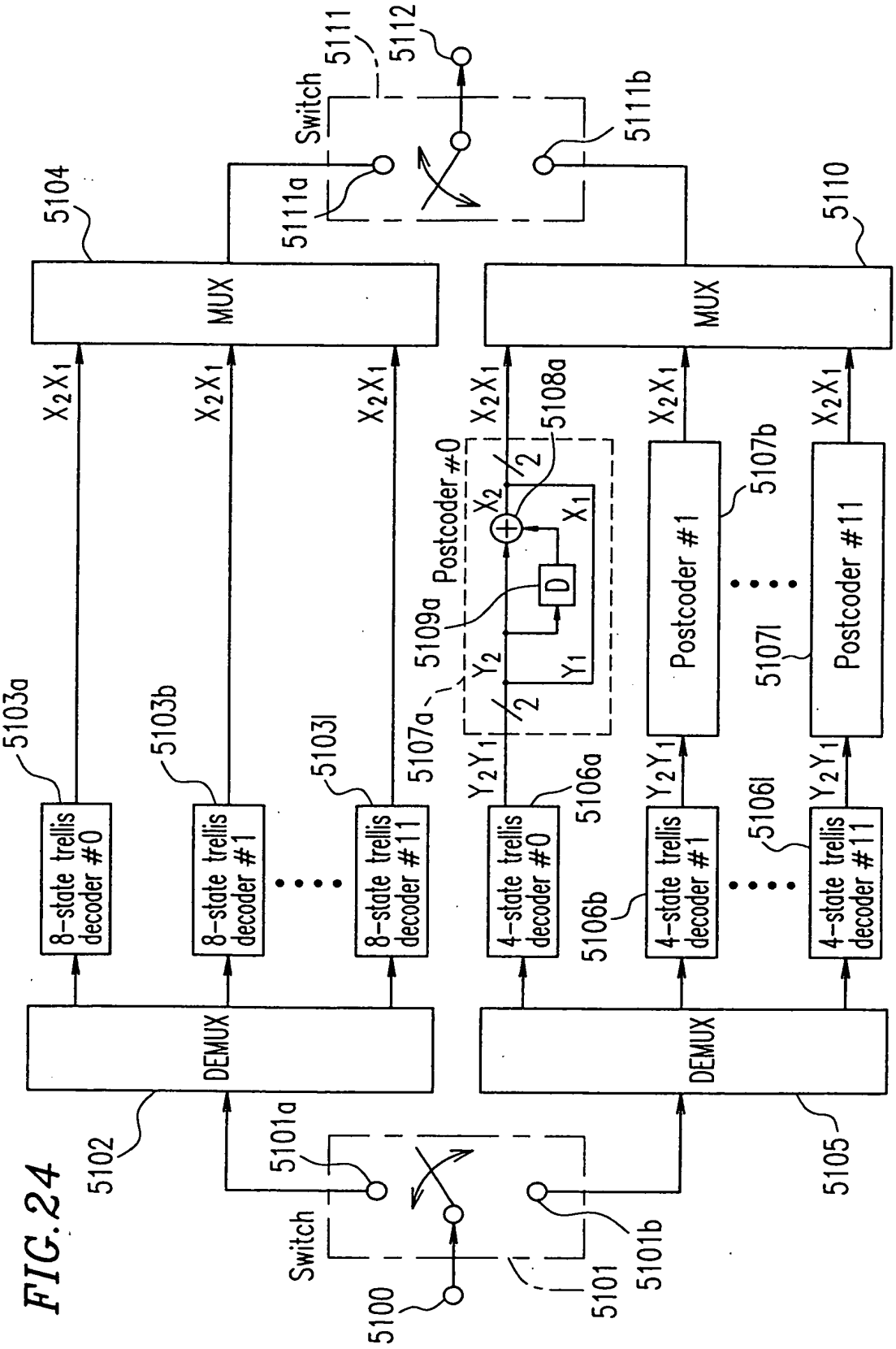


FIG. 24

Inventor(s): Hiroyuki Senda, et al.
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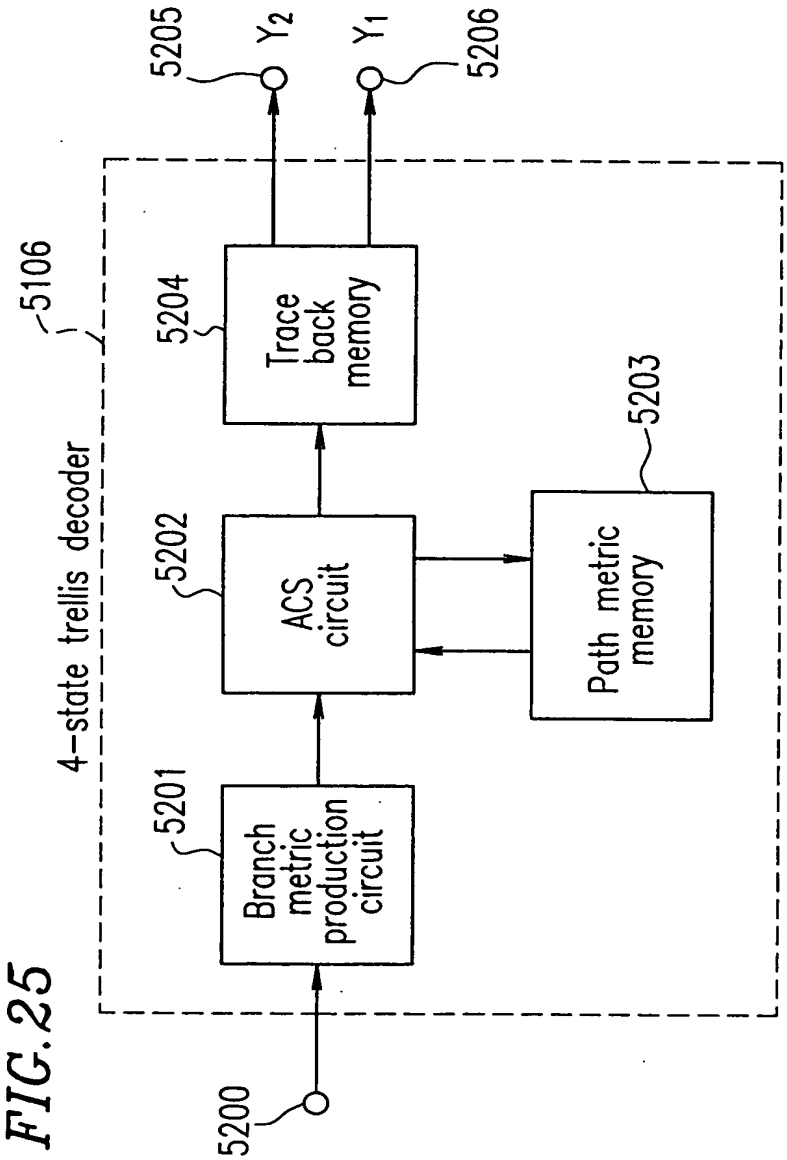

FIG.25

Inventor(s): Hiroyuki Senda, et al.
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Express Label No.: EV351884480US

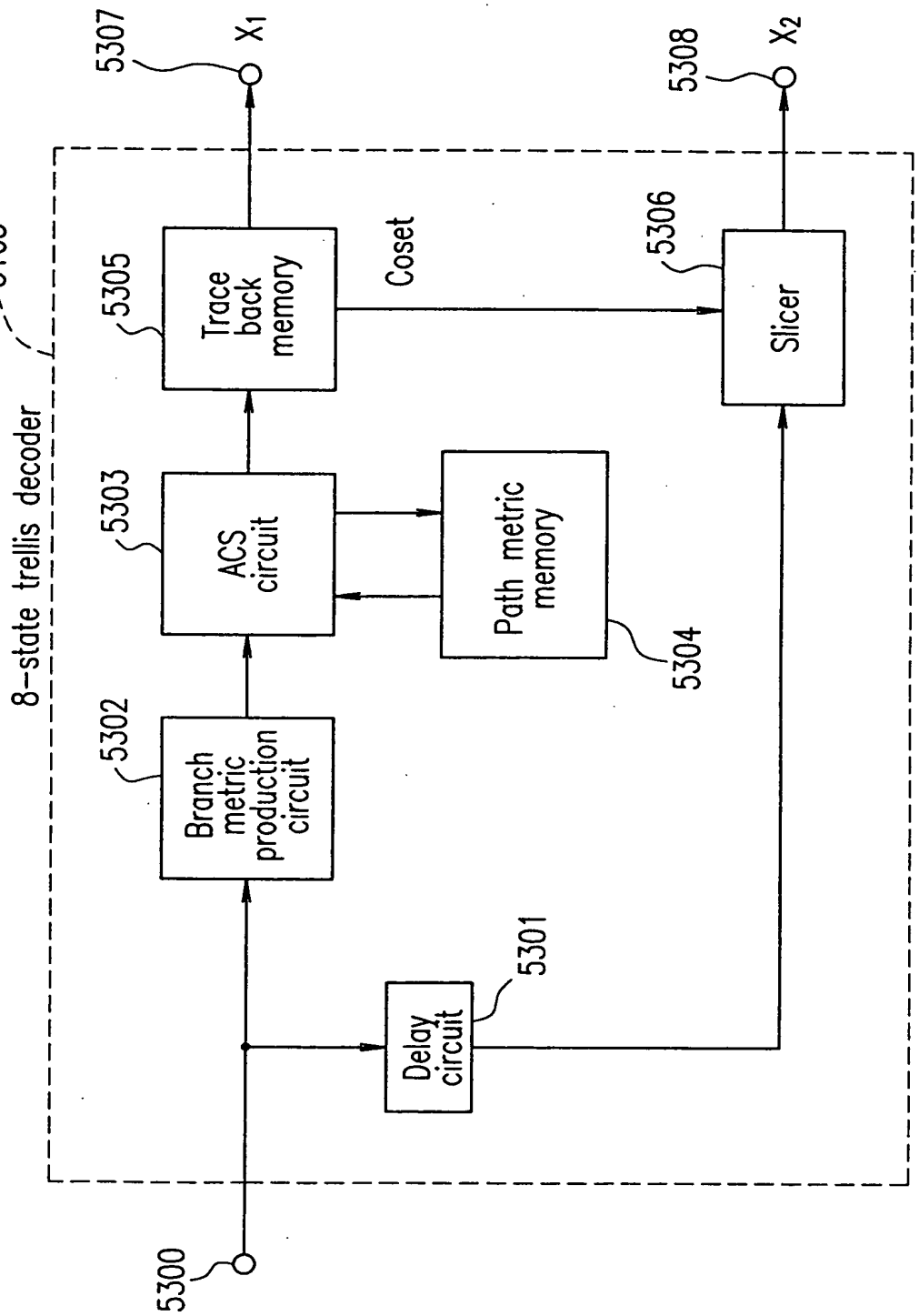

FIG.26

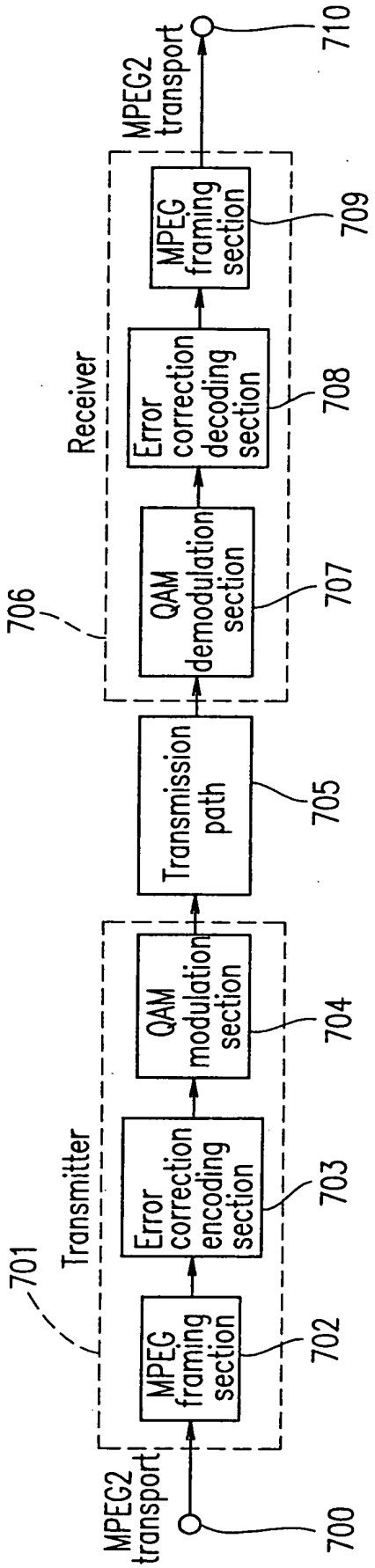
MPEG2 transport
700
Transmitter
701
MPEG framing section
702
Error correction encoding section
703
QAM modulation section
704
Transmission path
705
Receiver
706
QAM demodulation section
707
Error correction decoding section
708
MPEG framing section
709
MPEG2 transport
710

FIG. 27

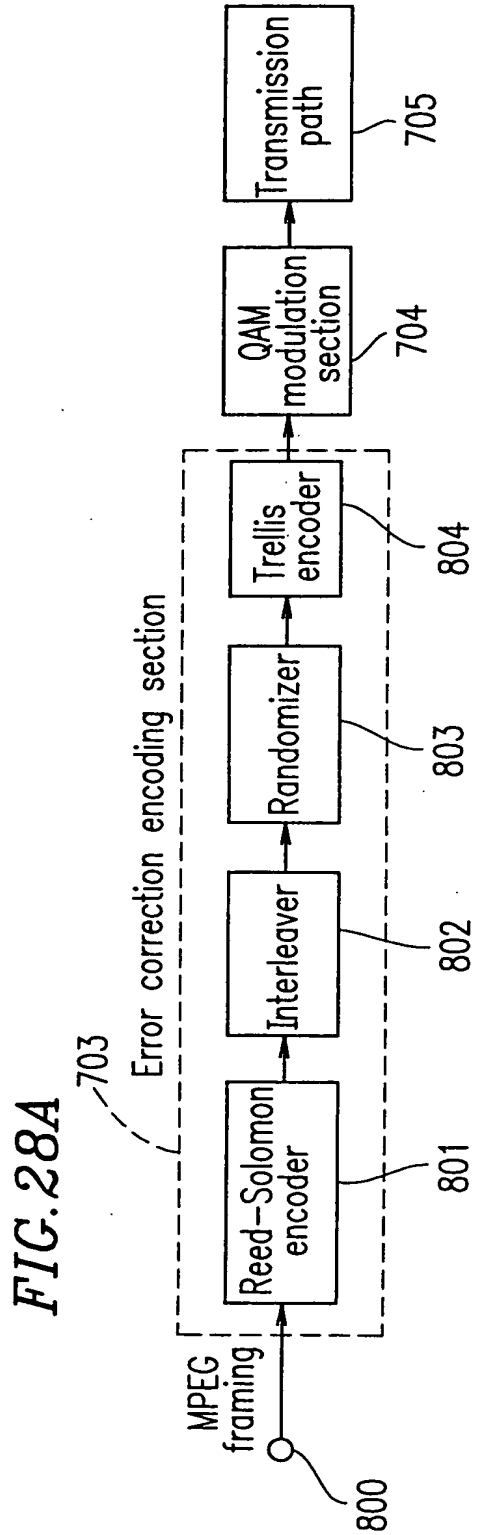
MPEG framing
800
Error correction encoding section
703
Reed–Solomon encoder
801
Interleaver
802
Randomizer
803
Trellis encoder
804
QAM modulation section
704
Transmission path
705

FIG. 28A

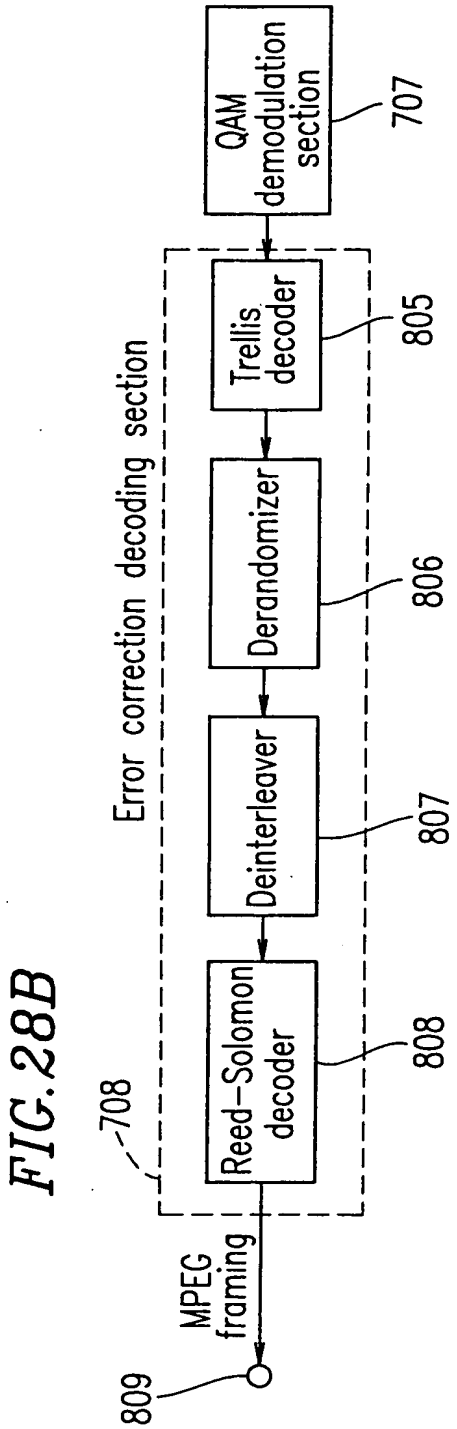
QAM demodulation section
707
Error correction decoding section
Trellis decoder
805
Derandomizer
806
Deinterleaver
807
Reed–Solomon decoder
808
708
MPEG framing
809

FIG.28B

Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

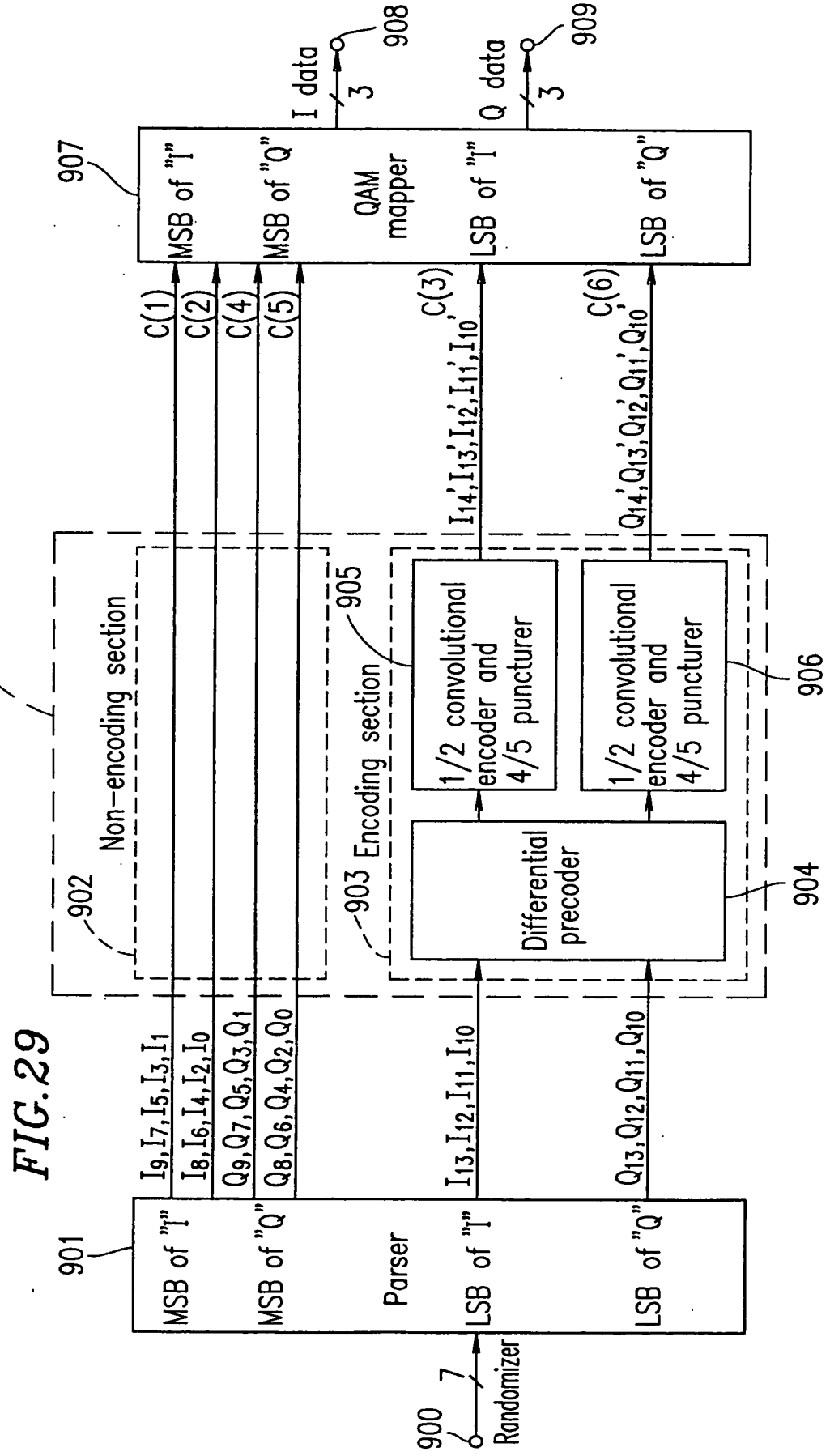

FIG.29

Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
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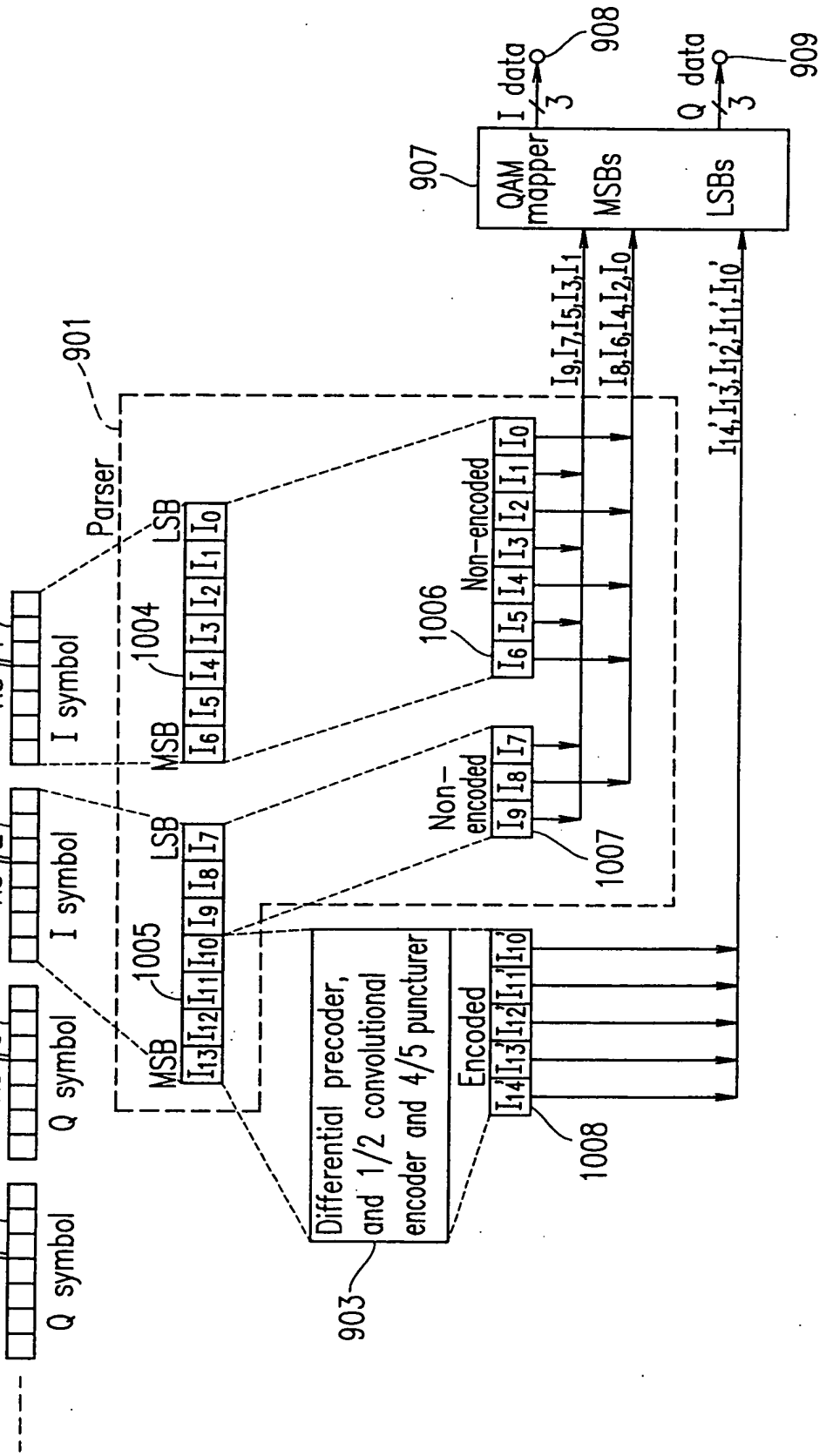
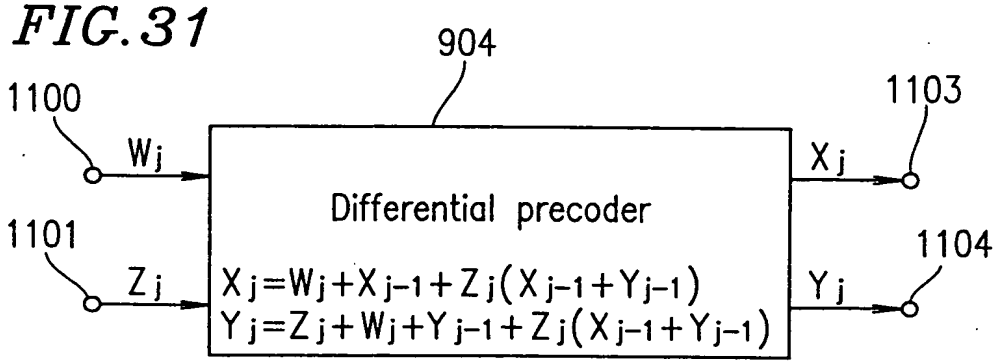
Express Label No.: EV351884480US

FIG. 30



Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

FIG. 31



Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

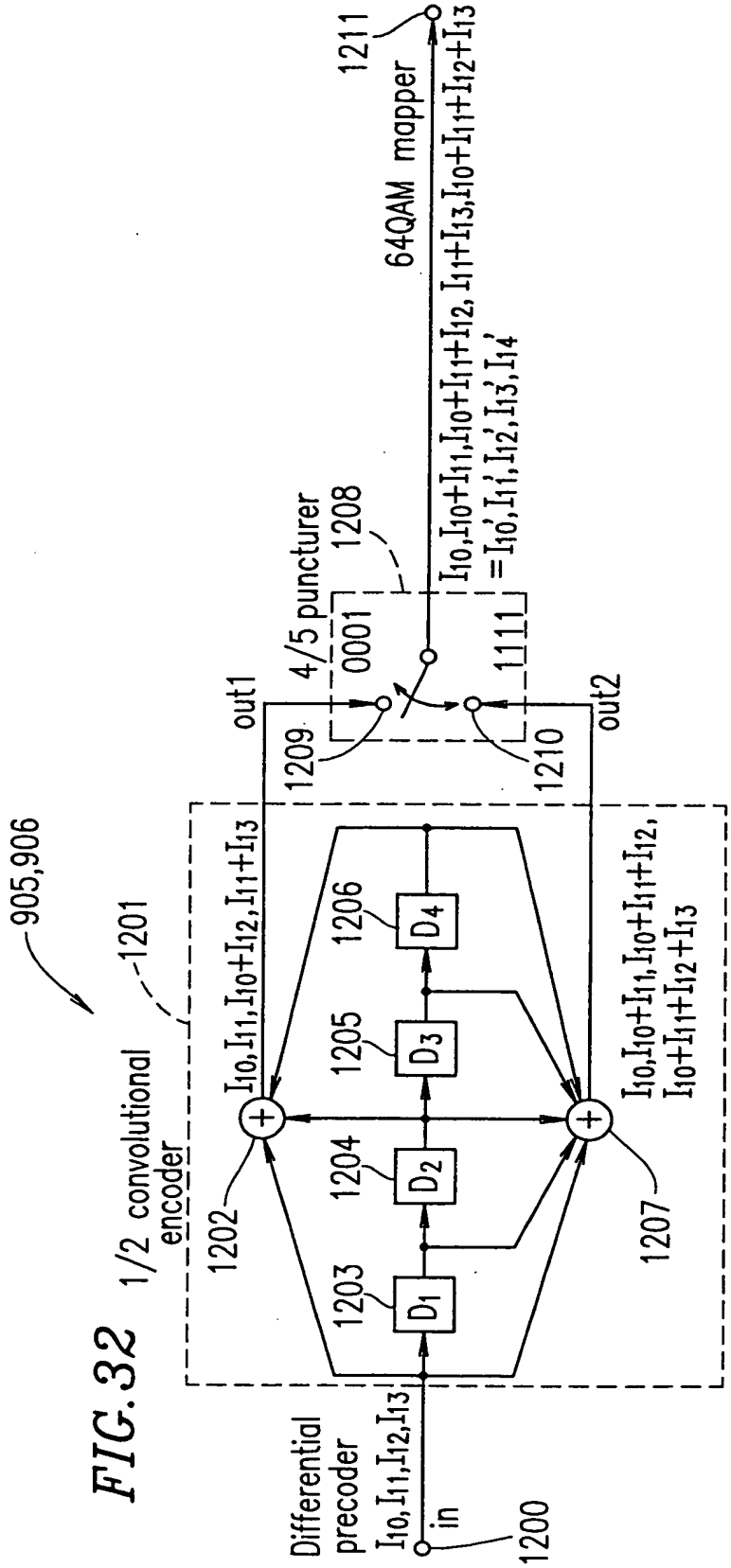


FIG. 32

FIG. 33A Arrangment of 64QAM encoding points

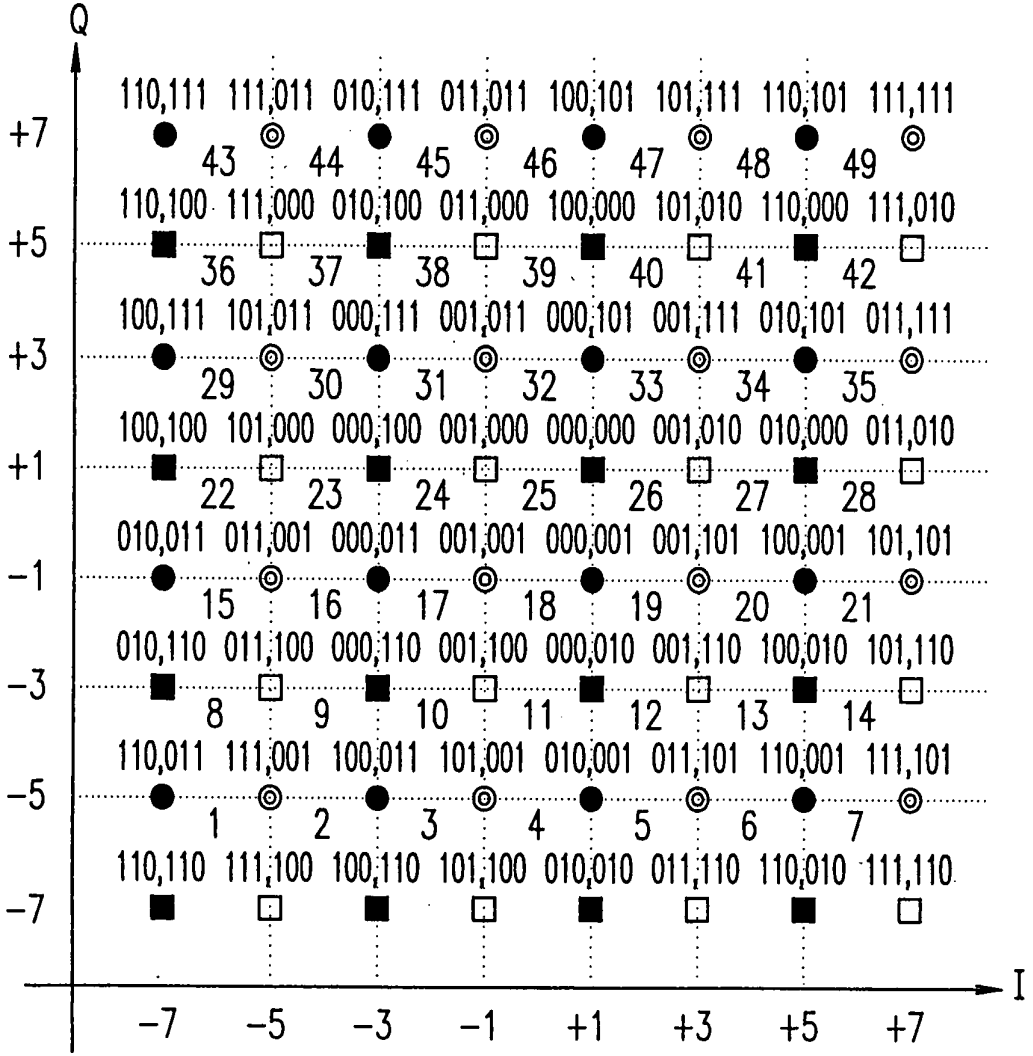


FIG. 33B

Encoding point

I bit			Q bit		
MSB					LSB
(C(1)	C(2)	C(3)	, C(4)	C(5)	C(6))

FIG. 33C

Encoded bits C(3),C(6)

	C(3)	C(6)
●	0	1
■	0	0
□	1	0
◎	1	1

"0"→ −7,−3,+1,+5

"1"→ −5,−1,+3,+7

Inventor(s): Hiroyuki Senda, et al.
Title: Error Correction Circuit and Error Correction Method
Customer No. 23122 Atty. Docket No. YAO-4210US1
Express Label No.: EV351884480US

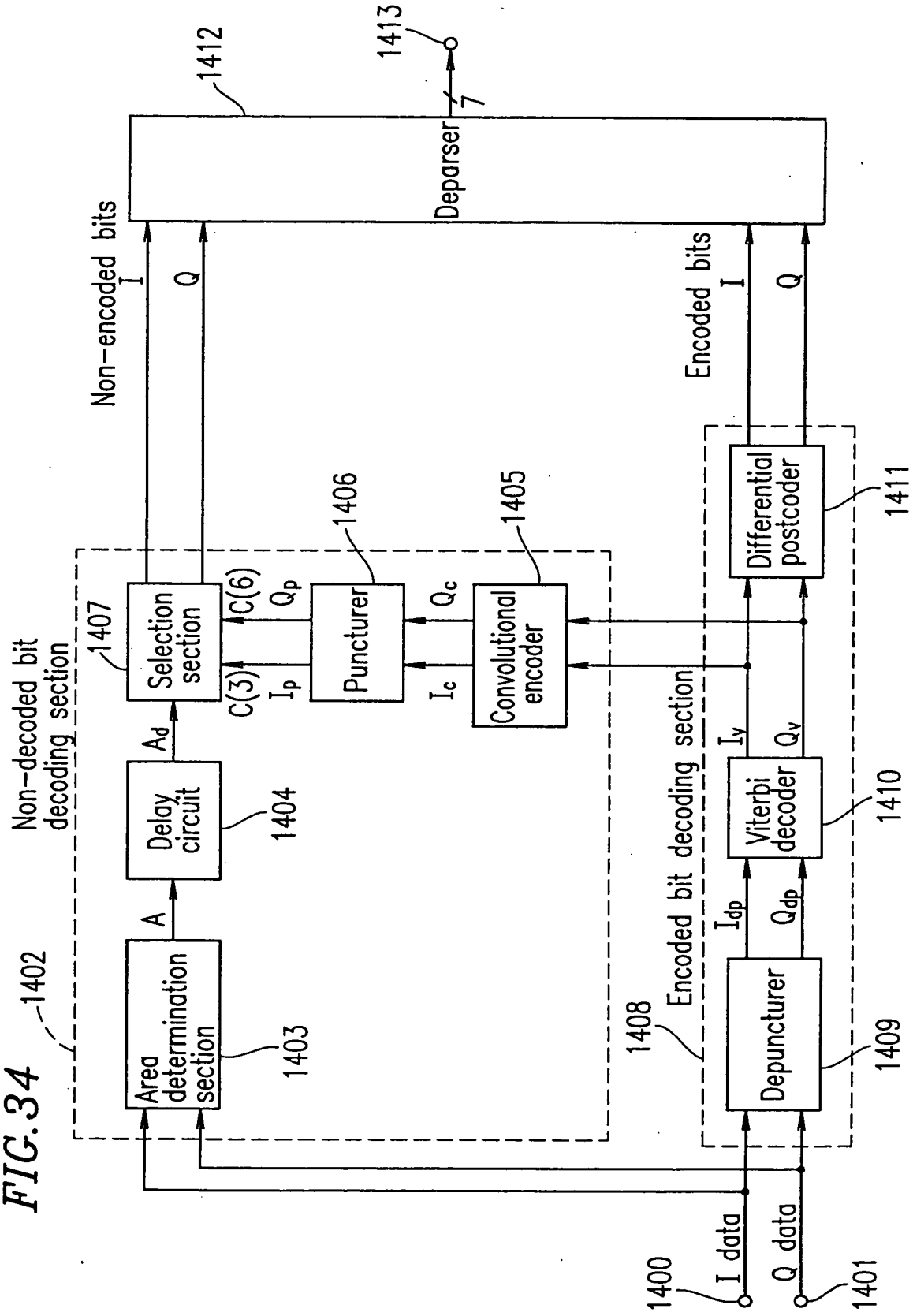

1412
1413
7
Deparser
Non-encoded bits
I
Q
Encoded bits
I
Q
Differential postcoder
1411
1406
1405
Puncturer
Convolutional encoder
Selection section
1407
C(6)
Qp
Qc
C(3)
Ip
Ic
Non-decoded bit decoding section
Ad
Delay circuit
1404
Iv
Qv
Viterbi decoder
1410
A
Area determination section
1403
1402
1408
Encoded bit decoding section
Idp
Qdp
Depuncturer
1409
I data
Q data
1400
1401

FIG. 34